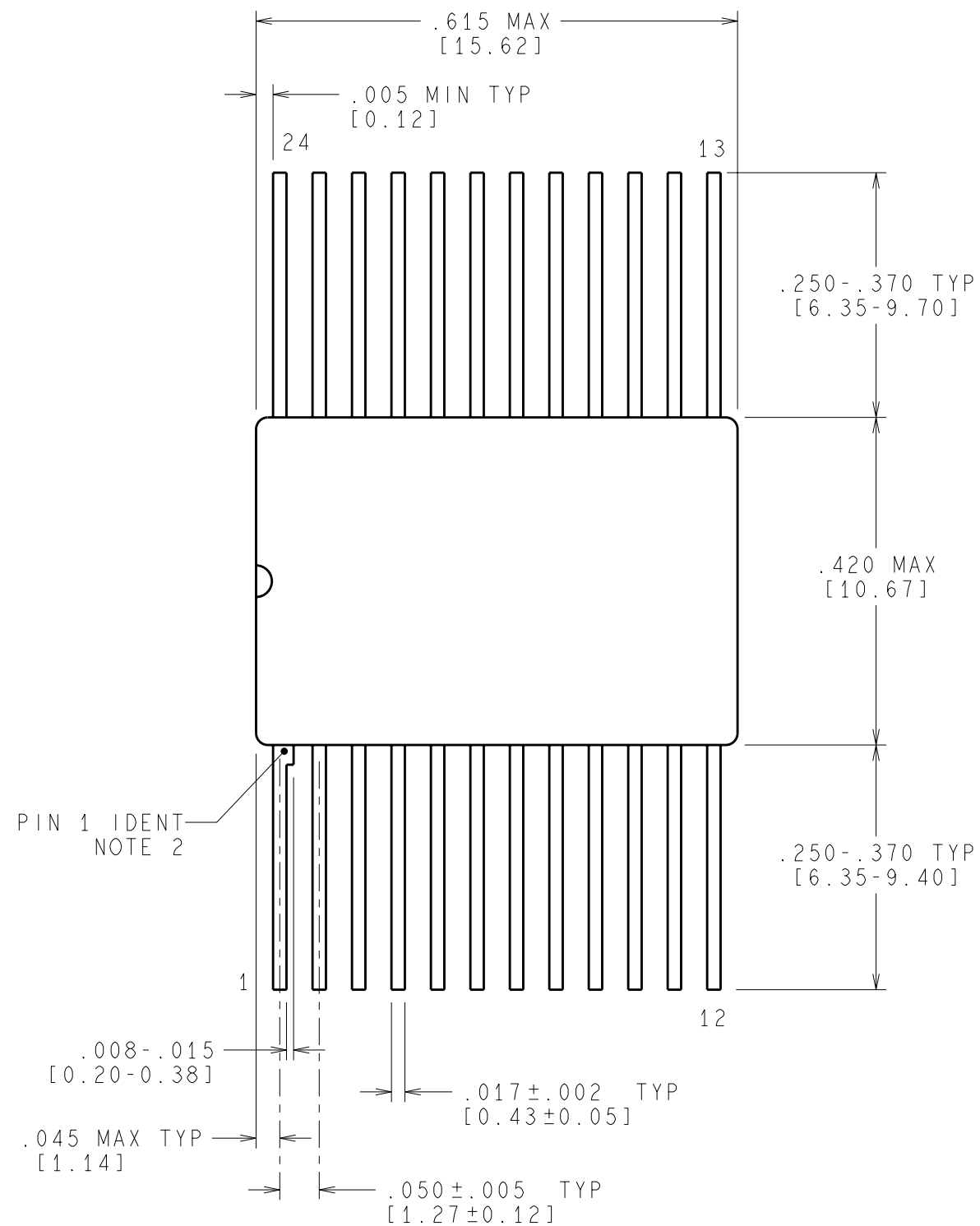
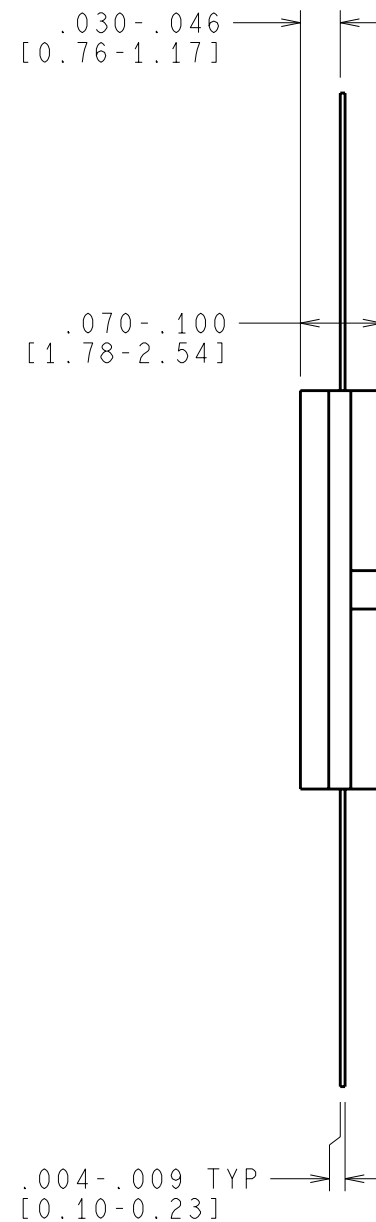


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE TITLE & MIL/AERO STAMP	11046	07/13/1995	MS/GY
G	LEAD THICKNESS WAS .005±.002; DELETE NOTE 2; TITLE & JEDEC NOTE; CHANGE TO B SIZE DWG FORMAT	1544	07/12/2004	TL/RW



PIN 1 IDENT
NOTE 2

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
- LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA.
 - A TAB ON LEAD 1, EITHER SIDE.
- REFERENCE JEDEC REGISTRATION MO-019, VARIATION AC.

CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE	National Semiconductor		
DRAWN MARTA SUCHY	07/13/1995	2900 Semiconductor Dr., Santa Clara, CA 95052-8090		
DFTG. CHK. MARTA SUCHY	07/12/2004	CERPACK, .420x.615x.100in, 24 LEAD, .05in PITCH		
ENGR. CHK. RANDY WALBERG	07/12/2004			
PROJECTION		SCALE	SIZE	DRAWING NUMBER
		NTS	B	(SC)MKT-W24C
FORMERLY: N/A		SHEET 1 of 1		REV G